Low-K Interconnect Stack with Thick Metal 9 Redistribution Layer and Cu Die Bump for 45nm High Volume Manufacturing

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Abstract

Interconnect process features are described for a 45nm high performance logic technology. Through extensive use of highly manufacturable carbon doped oxide low-k dielectric layers and aggressive scaling of the SiCN etch stop film the Metal-1 to Metal-8 interconnect stack demonstrates a 10% average capacitance reduction over the 65nm process. The interconnect stack also features a very thick Metal-9 layer to provide a low resistance path for the power and I/O routing. The combined interconnect stack provides high performance and reliability and supports a Pb-free 45nm process.

Introduction

As process dimensions continue to shrink, additional improvements are required to enable high performance logic devices. A full overview of the 45nm process has been given [1]. In this work the performance of the interconnect stack is detailed. The dual damascene processing scheme has been extended from previous generations with several improvements for increased performance.

To improve on-die power distribution a low resistance layer is used; this Thick Metal 9 (M9) redistribution layer is formed on top of the conventional on-die power distribution network. The M9 layer uses Cu plate-up between sacrificial photoresist lines followed by spin coating of a polymer dielectric. The M9 layer also improves C4 electromigration reliability by forming a low resistance path between neighboring C4 bumps on the same node.

The new process results in efficient power distribution with an environmentally friendly Pb-free die-package[2] and high performance on-die interconnects with robust reliability for high volume manufacturing.

Process Discussion

The on-die Metal-1to Metal-7 interconnects are formed by dual damascene patterning with highly manufacturable low-k CDO dielectrics. The lower layer metal pitches are 160nm, while upper layer metal pitches increase progressively to optimize density and performance as detailed in Table 1. M8 is also formed by dual damascene patterning but PECVD SiO_2 is used as the dielectric film and the M8 layer is covered with a thick PECVD silicon nitride film.

Instead of the dual damascene process used at the lower layers, M9 is formed using a plate up process. It begins by depositing a blanket Barrier/Seed (Ti/Cu) layer over the entire wafer. The M9 lines and spaces pattern is then created by using a thick photoresist. The patterned wafer is then put into a Cu electroplating bath where the M9 lines are plated. In the open areas (no resist) Cu lines will plate up with the resist lines acting as a mold. The resist is then stripped and the Barrier/Seed in between M9 lines is removed. The finished M9 lines are now capped with 400nm CVD nitride film to more robustly isolate them.

Table 1: Layer Material, Pitch, thickness and aspect ratio

Layer	Dielectric Material	Pitch (nm)	Thick (nm)	Aspect Ratio
Metal 1	Low k	160	144	1.8
Metal 2	Low k	160	144	1.8
Metal 3	Low k	160	144	1.8
Metal 4	Low k	240	216	1.8
Metal 5	Low k	280	252	1.8
Metal 6	Low k	360	324	1.8
Metal 7	Low k	560	504	1.8
Metal 8	SiO_2	810	720	1.8
Metal 9	Polymer	30.5µm	7µm	0.4

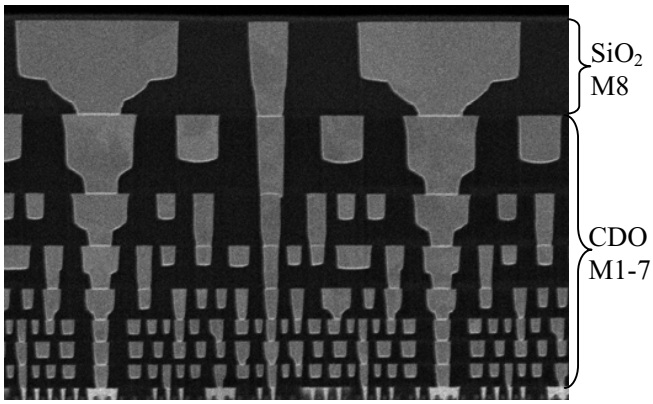

Fig. 1: SEM image of 45nm interconnect stack up to Metal-8

Now that the M9 Metal lines are formed and capped with nitride, the V9 dielectric is added by spinning on 16um of a spin-on polymer. Once the V9 openings are defined in the dielectric the wafers are put into a furnace to cure the material. From this point onwards the processing is very similar to that used to form the Cu bumps utilized in the 65nm process [3,4]. An SEM image of the M9 line, Via9 and base of the Cu bump can be seen in Figure 2.

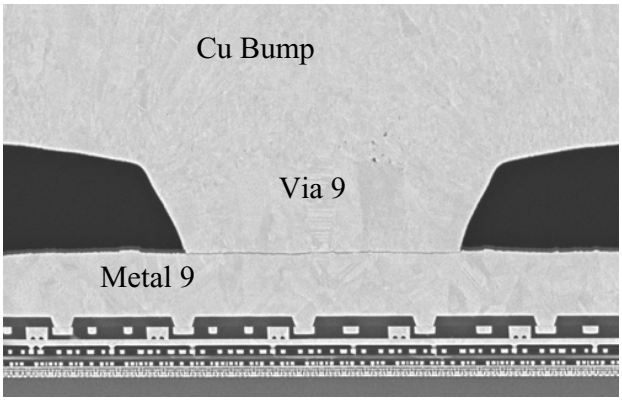

Fig. 2: SEM image detailing the Metal 9 and Via 9 Layers

Results

The 45nm process delivers reduced capacitance relative to the previous, 65nm [3], process generation through a combination of techniques. The newer process replaces SiO2 dielectric with low-k CDO dielectrics at M1, M6 and M7 for >20% capacitance improvement at those layers as shown in Figure 3. Also, at the lower metal layers, the SiCN etch stop layer is aggressively scaled for an additional 5% capacitance reduction. This scaling is shown in Figure 4; where the 25nm ES film can be clearly seen at the Metal-1 to Metal-3 layers.

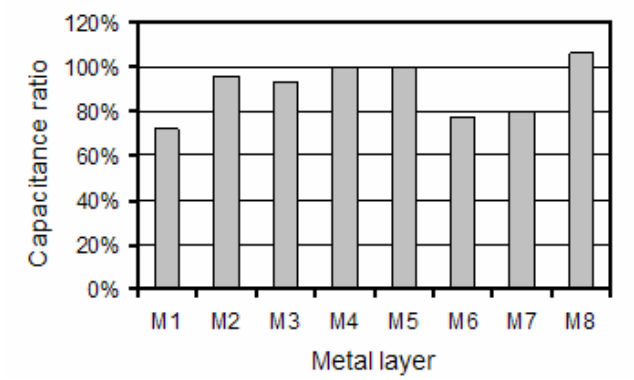

Fig. 3: Comparison of capacitance scaling at fixed length from Intel's 65nm to Intel's 45 nm processes.

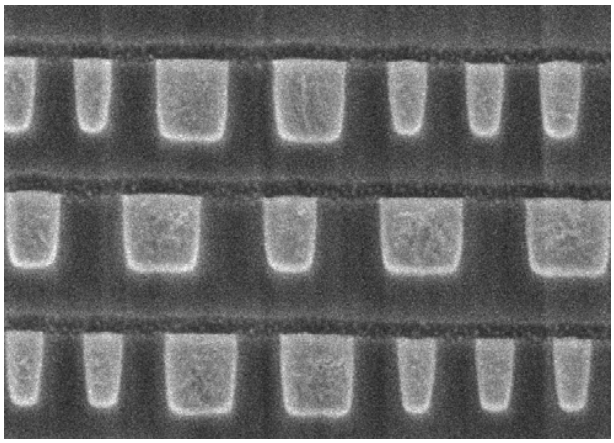
Figure 4. SEM of Metal-1 to Metal-3 layers showing the 25nm etch stop film.

Overall, the newer process achieves a 10% average capacitance improvement while re-using the robust CDO dielectric film and capital equipment from the previous process generation.

It is important to accurately benchmark interconnect RC performance. Interconnect capacitance and resistance are measured for minimum pitch lines with 50% dense, minimum-pitch metal patterns directly above and below the measured feature. Total capacitance is the sum of line-line capacitance and layer-layer capacitance as indicated in Figure 5.

Measured capacitance and resistance values for the 45nm process are shown in Figures 6 and 7 at the M2 and M6 layers, respectively. The M2 layer delivers median values of 0.20 fF/um total capacitance and 3.3 ohm/um resistance at 160nm pitch. Resistance at lower metal layers includes a 10% resistance penalty to enable high electromigration current density for high performance logic products. The M6 layer delivers median values of 0.21 fF/um total capacitance and 0.38 ohm/um resistance at 360nm pitch.

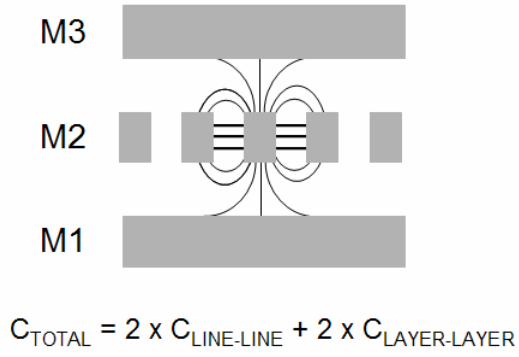

Fig. 5: Components of Capacitance measurement

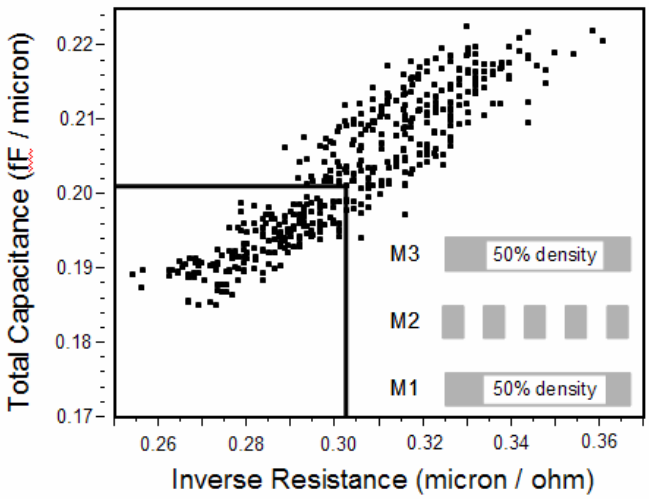

Fig. 6: Metal-2 R and C values measured at 160nm pitch with Metal-1 below and Metal-3 above, both at 50% density.

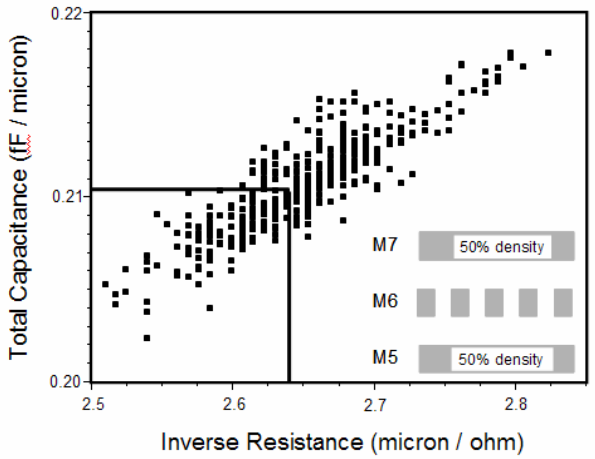

Fig. 7: Metal-6 R and C values measured at 360nm pitch with Metal-5 below and Metal-7 above, both at 50% density.

The thick M9 lines allows for neighboring bumps to be connected by a low resistance path to enable current redistribution upon initial electromigration damage at individual bumps. The large cross section area of M9 and its superb electromigration resistance achieves redundancy of neighboring bumps with no concern to the electromigration in M9 itself. Figure 8 shows an electromigration Time-to-Failure comparison between a single daisy chain of C4 bumps Vs. two daisy chains of bumps tested in parallel, connected through M9 with 2X of current; both tested under accelerated condition of higher temperature and high current. As the plot indicates, M9 redundant layout increases bump electromigration performance by at least 1.65X. Due to long testing periods the stress ended without any redundant links failing. This clearly shows M9 delivered the desired bump electromigration improvement.

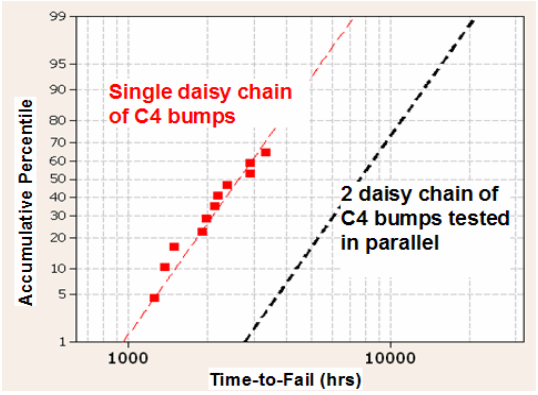

Fig. 8: Fail rate Cu Bumps chains with/without redundancy.

Figure 9 shows two Confocal Scanning Acoustic Microscope (CSAM) images of a Product units (full stack) taken after packaging with CuSnAg solder. Areas of cracking or interface delamination will show up as white or black spots apart form the contrast variation of the underlying pattern. The image on the left was taken after packing; no contrast areas are observed showing that the unit is free of cracking and/or interface delamination. These results have been reproduced in high volume and across the expected process variations. These results demonstrate that the 45nm process with its 7-layers of Low-k dielectrics has significant intrinsic margin to film cracking and interface delamination even with the increased stress of a Pb-free process.

It is critical that this thick M9 layer also be reliable in addition to having its electrical benefits. The image on the right side of Figure 9 shows a CSAM image of the M9/V9 layer after 25hours of HAST stress; clean of any delamination or cracking. The 45nm interconnect stack has been demonstrated to be capable of withstanding temperature shock, HAST and PreCon stresses all of which exceed end-of-life goals [5-7].

Summary

We have demonstrated an M1-M8 interconnect stack with a 10% average capacitance reduction over the 65nm process. This was done by the introduction of additional low-k layers and aggressive ES scaling. Additionally a thick M9 layer has been added to the interconnect stack to provide a low resistance path for the power and I/O routing.

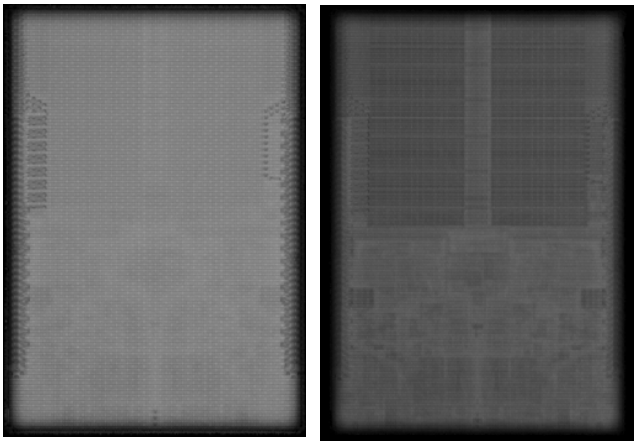
Fig. 9: CSAM images of production units. Image on left is post packaging and the image on the right is of a unit post 25-hours of HAST stress.

Acknowledgements

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